WHAT IS CLAIMED IS:

1. An arrangement of configurable logic blocks (CLB) in customer-specific circuits, the arrangement comprising:

an input data node for carrying input data;

a CLB control logic circuit having a first input, a second input, a third input, a fourth input and an output;

at least one look-up table in which a switching function of at least one conditional branch is implemented with content addressability, wherein the at least one look-up table generates an "if then else" branch that realizes a comparison of the input data with comparison data previously stored in the at least one look-up table, and wherein a result output of the at least one look-up table is provided to a third input of the CLB control logic;

an input data bus coupled between the input data node and a bus input of the at least one look-up table, wherein the first input of the CLB control logic circuit is coupled to the input data node via the input data bus;

at least one multiplexer having a control input coupled to the input data node and also to the first input of the CLB control logic circuit via at least part of the bit width of the input data bus, an output of the at least one multiplexer being coupled to a fourth input of the CLB control logic;

a control input node coupled via a control bus to the second input of the CLB control logic; and

at least one register data bus coupled between a register data bus output of the at least one look-up table and a bus input of the at least one multiplexer.

2. The arrangement of claim 1, wherein the at least one look-up table (2), (12) is realized with the conditional branch implemented in it by such a switching function, and wherein the at least one look-up table (2), (12) comprises:

a register which stores the comparison data; and

a comparator coupled to the input data node and the register, the comparator operable to compare the input data with the comparison data.

3. The arrangement of claim 2 wherein the bus input of the at least one look-up table is coupled to a first bus input of the comparator and wherein a bus output of the register (4), (14) is coupled to a second bus input of the comparator and also to the register data bus output of the at least one look-up table, and wherein an output of the comparator is coupled to the result output of the at least one look-up table.

4. The arrangement of claim 1 wherein the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

5. The arrangement of claim 1 wherein the output of the CLB control logic serving as an output of the CLB.

6. A logic circuit comprising:

a register;

a comparator with a first input coupled to the register and with a second input coupled to an input node;

a multiplexer with an input coupled to the register; and

a control block with inputs coupled to the multiplexer, the comparator, the input node and an input control node, wherein the logic circuit realizes an "if then else" branch based upon information carried at the input node and information stored in the register.

7. The circuit of claim 6 wherein the logic circuit comprises a configurable logic block.

8. The circuit of claim 7 wherein the configurable logic blocks are realized in Field Programmable Gate Array (FPGA) technology.

9. The circuit of claim 6 and further comprising:

a second register;

a second comparator with a first input coupled to the second register and with a second input coupled to the input node;

a second multiplexer with an input coupled to the second register; and

wherein the control block is coupled to the second comparator and the second multiplexer.

10. The circuit of claim 6 wherein the output of the CLB control logic serving as an output of the logic circuit.

11. A logic circuit comprising:

means for performing a switching function of at least one conditional branch is implemented with content addressability, wherein the means for performing a switching function generates an "if then else" branch that realizes a comparison of input data with previously stored comparison data;

means, coupled to the means for performing a switch function, for selecting at least a portion of the comparison data; and

a CLB control logic circuit having a first input coupled to receive at least a portion of the input data, a second input coupled to the means for performing a switching function, and a third input coupled to the means for selecting.

12. The circuit of claim 11 wherein the means for performing a switching function comprises:

means for storing the comparison data; and

means for comparing the comparison data and the input data.

13. The circuit of claim 11 wherein the means for performing a switching function comprises:

a register that stores the comparison data; and

a comparator coupled to the register and to an input data node that carries the input data.

14. The circuit of claim 1 wherein the logic circuit is realized in Field Programmable Gate Array (FPGA) technology.